

(19) World Intellectual Property  
Organization  
International Bureau



(43) International Publication Date  
29 January 2004 (29.01.2004)

PCT

(10) International Publication Number  
**WO 2004/010470 A2**

- (51) International Patent Classification<sup>7</sup>: **H01L**
- (21) International Application Number:  
PCT/US2003/022318
- (22) International Filing Date: 17 July 2003 (17.07.2003)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:  
60/397,554 22 July 2002 (22.07.2002) US
- (71) Applicant (for all designated States except US): **UNIVERSITY OF HOUSTON** [US/US]; 4800 Calhoun Road, Houston, TX 77204-2015 (US).
- (72) Inventors; and
- (75) Inventors/Applicants (for US only): **CHU, Wei-Kan** [US/US]; 4800 Calhoun Road, Houston, TX 77204 (US). **SHAO, Lin** [CN/US]; 4800 Calhoun Road, Houston, TX 77204-2015 (US). **LIU, Jiarui** [US/US]; 4800 Calhoun Road, Houston, TX 77204-2015 (US).
- (74) Agents: **HEADLEY, Tim** et al.; Gardere Wynne Sewell LLP, 1000 Louisiana, Suite 3400, Houston, TX 77002-5007 (US).

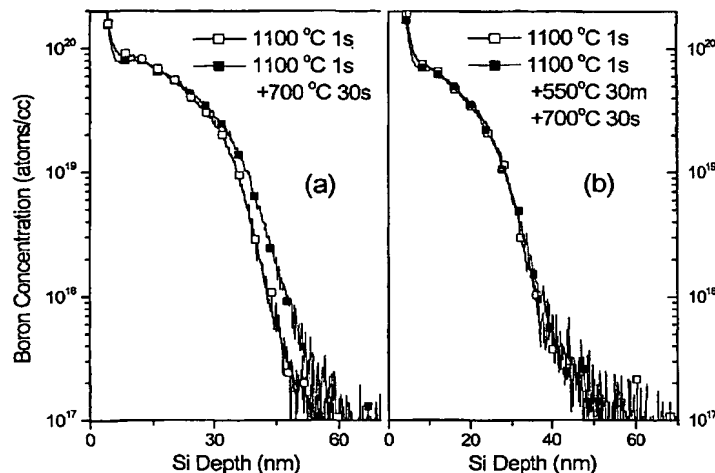
- (81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.
- (84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

#### Declarations under Rule 4.17:

- as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for the following designations AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH,

[Continued on next page]

(54) Title: METHOD TO OVERCOME INSTABILITY OF ULTRA-SHALLOW SEMICONDUCTOR JUNCTIONS



(57) Abstract: A method of forming a stable junction on a microelectronic structure on a semiconductor wafer having a silicon surface layer on a substrate includes the following steps: implanting dopant ions into the surface layer; cleaning and oxidizing the surface layer, and twice annealing the wafer to recover a damaged silicon crystal structure of the surface layer resulting from the low energy ion implantation. The first annealing process uses a temperature range of 800°C to 1200°C for a duration from about a fraction of a second to less than about 1000 seconds, with a ramp-up rate of about 50°C/second to about 1000°C/second. The second annealing process uses a temperature range of 400°C to 650°C for a time period of from about 1 second to about 10 hours, and more preferably, from about 60 seconds to about 1 hour. Both annealing processes include cooling processes.